Ultra-Low Power, Radiation Tolerant, Reconfigurable Field Programmable Gate Array (FPGA) Technology Development†

Earl Fuller[1], Brian Smith[2]
PicoDyne Inc.
[1] 10500 Research Rd SE, Albuquerque, NM 87123-3400
[2] 1918 Forest Drive, Annapolis MD 21401-4319

Abstract – **On-orbit reconfigurable computing offers system design flexibility long sought after. In additional, ultra-low power (ULP) electronics is an enabling technology for system miniaturization and thereby cost. Two core capabilities are being developed, namely RT (radiation tolerant) technology and ULP CMOS process technology. RT technology enables radiation tolerant CMOS integrated circuits to be fabricated at commercial foundries. ULP process technology allows the operation of high performance active digital circuits at a greatly reduced level of power, by operating with supply voltages of 0.5 volts or less with as much as 100 times reduction in power consumption. Circuits are being developed compatible with existing FPGA software tools.**

I. Introduction

Programmable logic has advantages over ASIC designs for the space community, including: reduced cost, faster and cheaper prototyping, and reduced lead-time before flight. Reprogrammable logic offers the additional benefit of allowing on-orbit design changes. This flexibility allows a mission to adapt systems to evolving requirements. For remote sensing applications, computing system payloads may be used for multiple sensors, multiple targets, and multiple modes. Such reuse reduces the weight, space, and power requirements. In addition, the payload can be updated as signal-processing techniques improve throughout the mission lifetime. The underlying electronic component technology required to achieve this capability is Field Programmable Gate Arrays (FPGA).

FPGAs provide an array of logic resources, which may be interconnected, and configured for specific functions. All logic definitions and block connections are controlled by a programmable interconnection method that varies depending on the technology chosen. One-time programmable methods include fusing links and reconfigurable methods utilize either EEPROM or SRAM cells. Despite their volatility, SRAM cells are preferred for reconfiguration due to speed advantages and process simplicity.

ASIC devices provide the advantage of "instant-on". They do not require an initial configuration cycle before becoming functionally active after power-up. An FPGA requires a configuration cycle after power-up to be functionally active. However, many devices utilize a high-speed configuration interface, which can bring the device functionally active within 20ms after power-up. The re-programmability and readback capability of FPGAs allows for the functional description of the device to be altered an unlimited amount of times which allows for functional evolution throughout the mission life span. Additionally, the mission life span itself may be increased by this capability. If any portion of the logic array is rendered inoperable, the required functional design can be re-implemented to not utilize the effected area of the device and remotely transmitted to the spacecraft/application.

There are two fundamental challenges for the use of FPGAs in space applications. First, the devices must be able to withstand the effects of ionizing radiation and energetic particle-induced upset (commonly referred to as Single Event Effects (SEE) such as Single Event Upset (SEU) and Single Event Latch-up (SEL)). And second, there must be an emphasis on low power consumption, without compromising performance, because of space power limitations and thermal management. Solving both of these challenges is essential to meeting the future system requirements for small satellite systems, sensorcraft, and eventually sensorwebs This paper will discuss an FPGA technology being developed that will directly address these issues.

II. Ultra-Low Power Technology

A reduction in operating voltage is key. Modern semiconductors use power supply voltages of from 5 volts down to 1.6 volts, with each process having its unique benefits and compromises. When a part is active (i.e. switching), power is proportional to the square of voltage, so reducing voltage has a very significant effect on power. A 5-volt part for example would use at least 100 times more power than a 0.5-volt part. To maintain performance (speed) at this lower voltage the transistor threshold voltage needs to be scaled down accordingly. The challenge exists because when threshold is lowered, leakage currents increase and standby power can increase. Traditionally, semiconductors have been designed for standby power to be 1/1000th of active power, or less. This results in low battery consumption in a device when it is not in use. The ULP approach is to develop

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devices that reduce power consumption when a device is in use, and accordingly balances the tradeoff between slightly higher leakage currents with lower transistor thresholds and operating voltages to achieve a situation where active and standby power are roughly equal. In this way total power is reduced, and in particular, power is as low as it can be without compromising performance when the device is actually operating.

Power is primarily the average of active power and standby power. Performance, or speed of operation, is primarily determined by the ratio of transistor threshold voltage to the supply voltage.

When a circuit is active, transistors are switching and the result is charging and discharging of capacitance at various circuit nodes. The important equation is the dynamic power dissipation of a circuit, which is:

$$P_d = \text{frequency} * C_{load} * V^2$$

Where P_d = Dynamic power dissipation
frequency = operating frequency
C_{load} = load capacitance
V^2 = the square of the operating voltage

Given three terms in this equation, there are three separate opportunities to reduce dynamic power. One can always reduce power by reducing frequency. After all, the most common low power circuit is in a wristwatch; it lasts for years, but it is not a very high performance circuit. However, most systems require no compromise in performance so frequency reduction is not pursued.

Another means to reduce power is to reduce circuit capacitance, C_{load}. The semiconductor industry commonly pursues this technique by constantly shrinking technology in fabrication. Process advancements in smaller feature size reduces the device area, therefore capacitance, therefore the dynamic power dissipation of individual circuit elements. Many other process-engineering details are implemented to reduce the total C_{load} per circuit element. Generally, with reduction of feature size comes increased integration, so while the power dissipation of the individual transistor is reduced, the power of the entire chip remains the same or even increases. Much of this benefit is achieved only after significant investment in sub-micron wafer fabrication facilities.

The potential power reduction with reduced voltage is enhanced by the squaring of the V term in the equation. This is the principal focus for a ULP FPGA, because it has the most benefit in power reduction for the least cost.

The important equation for standby power is:

$$P_s = V * I_{leakage} = V * e^{-V_{th}/kT}$$

Where P_s = Standby power dissipation
V = the operating voltage
$I_{leakage}$ = transistor leakage current

And

V_{th} = threshold voltage for the transistors
kT = a constant times temperature

In this case, power decreases linearly with operating voltage but increases exponentially as transistor threshold voltage decreases. Accordingly, ULP modifies the transistors to achieve thresholds near 0 volts. Then, a back-bias voltage is added to be able to allow the transistors to be able to function both on and off. There is an increase in leakage current resulting in increased standby power. However, the increase in standby power is more than compensated by the significant decrease in active power.

The draw back to reducing power by reducing voltage is that in conventional circuits, reducing voltage also reduces performance (speed). In deep sub-micron technologies, where short channel effects dominate the transistor saturation current, the switching speed of a logic gate is a strong function of the ratio of V_{th} / V, but is a very weak function of the actual magnitude of V. Therefore performance can be maintained even with decreasing supply voltage if there is also a corresponding decrease in threshold voltage. This is what ULP does. However, conventional thinking considers that there is a practical limit to threshold reduction because with threshold reduction comes an increase in off-transistor leakage current, which increases static power consumption. Further, any CMOS technology that does not include an active means for adjusting the transistor thresholds must also be over-designed to account for manufacturing variation and environmental conditions. The need for an overly conservative design limits the potential power supply voltage reduction, and ULP technology solves this concern.

In order to remain on its historical productivity advancement path the semiconductor industry must make increasing large investments in both capital and R&D. To coordinate these massive investments cooperative programs such as SEMATECH must play an active role. To that end, the Semiconductor Industry Association (SIA) brought together technology leaders from industry, government, and universities to create the SIA's 2000 International Technology Roadmap for Semiconductors. This roadmap adopts a 15-year horizon and seeks to forge a national consensus on the research needs of industry. The minimum logic supply

voltage targets established in the Overall Roadmap Technology Characteristics (ORTC) tables are:

TABLE 1.
SIA Technology Roadmap, 2000 Update

Year	Operating Voltage Range (volts)
1997	1.8-2.5
1999	1.5-1.8
2001	1.2-1.5
2003	0.9-1.2
2005	0.8-1.1
2011	0.5-0.6

A primary feature of the ULP technology is that it enables 2011 operating voltages for devices fabricated on today's commercial wafer fabs. Measurements made on a device designed conventionally to operate at 3.3 volts and the same device using ULP technology at 0.5 volts demonstrated a 49 times reduction in dynamic power despite a 12 times increase in static power. Overall, power dissipation is lower so long as the duty cycle of the part is greater than 1%. The chart below indicates the comparison.

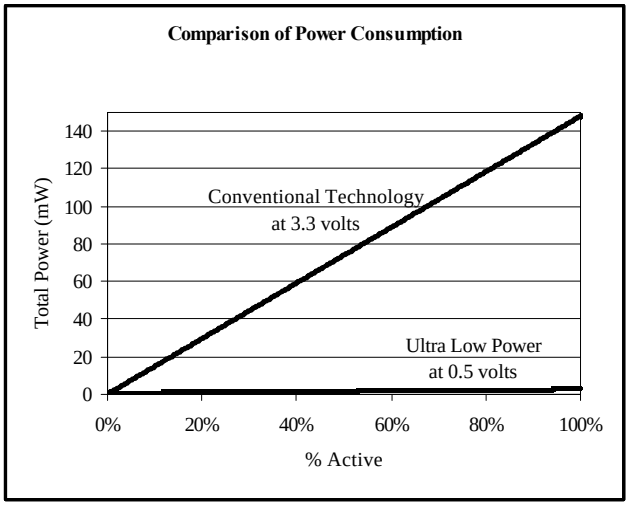

Figure 1. Power consumption measurements of the same device, operating at the same frequency, showing the significantly lower power consumption of ultra-low power technology.

Although the ULP operating voltages are low, the operating currents are not; consequently, noise propagation is not thought to be a significant issue with ULP. Internal noise sources scale at least as fast as the supply voltage. Capacitive coupled noise scales as voltage, resistively coupled noise as V^2, and inductively coupled noise as V in the short-channel limit and as V^3 in the long-channel limit. Thermal noise does not scale but is only about 100 μV. Relative noise margins tend to degrade with aggressively scaled thresholds but are still large enough to support a broad range of logic styles.

III. Radiation Tolerance

The space radiation effects of most importance for this work are tolerance to total ionizing dose, and single event effects including latch-up and upset.

A. Total Ionizing Dose Tolerance

One unanticipated benefit of ULP technology is a significant hardening of the devices against total dose effects. Measurements indicate an improvement in total dose immunity from only 25 krads in the regular voltage process up to better than 200 krads in the equivalent ULP process fabricated on the same line [1]. The application of back-bias greatly improves the radiation tolerance. The most important physical effect is the resulting increase in threshold voltage in the field oxide and edge regions of the channel.

The fabrication facility chosen to develop this process and evaluate the total ionizing dose benefit is the 0.35μm bulk CMOS process line at American Microsystems, Inc. (Pocatello ID). This process uses Local Oxidation of Silicon (LOCOS) isolation and has no special steps to improve the radiation tolerance. Since most satellite applications require total ionizing dose tolerance at or below the 200 krads level measured, ULP technology should be widely applicable.

B. Single Event Effects

Radiation mitigation techniques that were developed at the Microelectronics Research Center (MRC) and the University of New Mexico have been licensed for application to this FPGA development. These techniques were originally perfected under NASA sponsorship and include guard banding for latchup protection and special circuit techniques to mitigate against the effects of SEUs. The MRC approach has been implemented in a number of different process technologies at regular voltage and has been extensively tested at the Brookhaven Heavy Ion Facility. These techniques are shown to eliminate latchup and to prevent SEUs below an LET of 120 MeV-cm^2/mg. Devices using these technologies are successfully flying in a number of missions. The application of these techniques to ULP is seen as a natural scaling process, with no anticipated problems. In fact, operating at 0.5 V, the possibility of latchup is virtually eliminated without special techniques, although it will be necessary to protect the higher voltage bias circuits that are used to control ULP operations. ULP devices have been fabricated using the SEU protection circuit techniques, and they have been found to operate normally. The significant enhancement of the very low LET threshold of the SRAM based FPGA provides substantial benefit to satellite

applications by mitigating SEUs without eliminating reconfigurability.

Previous work [2] has shown that commercial SRAM-based FPGA's have a very low upset threshold as indicated by the following sample chart:

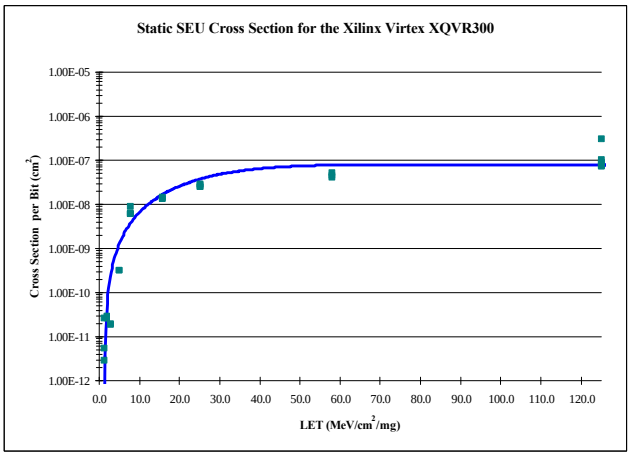

Figure 2: Static heavy ion bit upset cross-section vs. LET for the *Virtex* FPGA.

The heavy ion cross-section of the device shown in figure 2 is typical of modern sub-micron commercial SRAM technologies. Low energy ions, as well as protons, which dominate the radiation environment for earth orbiting satellites, are able to cause upsets frequently, as the Figure 3 below summarizes [3].

Application of radiation-hardened circuits to this type of FPGA would significantly increase the upset threshold and virtually eliminate the upset rates that are so significant in Figure 3.

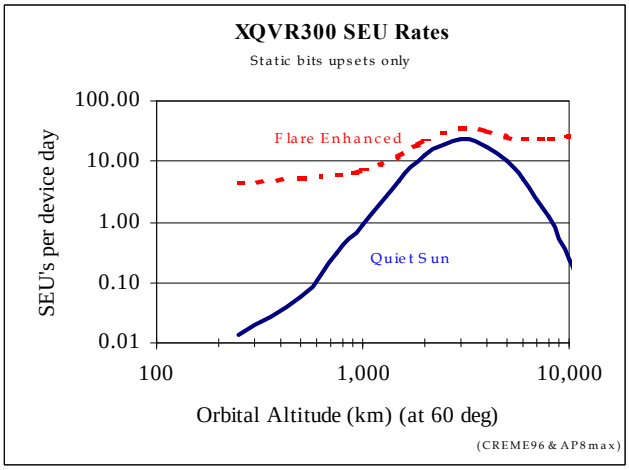

Figure 3: This plot is obtained by calculating the hypothetical sensitive volume of the Exiling Virtex XQVR300 as the product of all of the bits in the FPGA and the average cross-section from figures 2 and proton cross-section in the referenced document.

IV. Selection of FPGA to be Cloned

Since is essential that an FPGA be developed along with a suite of CAD software tools that enable convenient design implementation, it is important to develop a device for which software already exists. The best alternative is the XC6200 High-Performance Sea of Gates FPGA formerly supplied by Xilinx Inc. Design software is already available and there are hardware development platforms that exist in the marketplace. Accordingly, this program could focus on semiconductor technology development to demonstrate the efficacy of the radiation tolerant and ultra low power methods. Even though a discontinued product from Xilinx, heritage products still exist for direct comparison to ULP version.

The XC6200 is a family of fine-grain, sea of gates FPGA's. These devices are designed to operate in close co-operation with a microprocessor or microcontroller to provide an implementation of functions normally placed on an ASIC. These include interfaces to external hardware and peripherals, glue logic, and custom coprocessors, including bit-level and systolic operations unsuited to standard processors. The family was produced with 16k gates and 64k gates, which meets the minimum level of integration to be useful in system designs.

An XC6200 part is composed of a large array of simple configurable cells. Each basic cell contains a computation unit capable of simultaneously implementing one of a set of logic level functions *and* a routing area through which inter-cell communication can take place. The structure is simple, symmetrical, hierarchical and regular, allowing even novice users to quickly make efficient use of resources available.

The implementation of radiation tolerant circuits design methods and an ultra-low power process requires a detailed understanding of the basic cell, and function unit. Once detailed schematics are extracted from the existing design, circuit substitutions will be made to achieve the goals of the program.

The basic cell is shown in figure 4 and the details of the function unit are shown in figure 5. Bits within the configuration memory control the multiplexers within the cell. The design of the function unit uses the fact that any function of two Boolean variables can be computed by a 2:1 multiplexer if suitable values chosen from the input variables and their counterparts are placed on its inputs. Figure 6 shows the schematic representations of the basic cell functions possible.

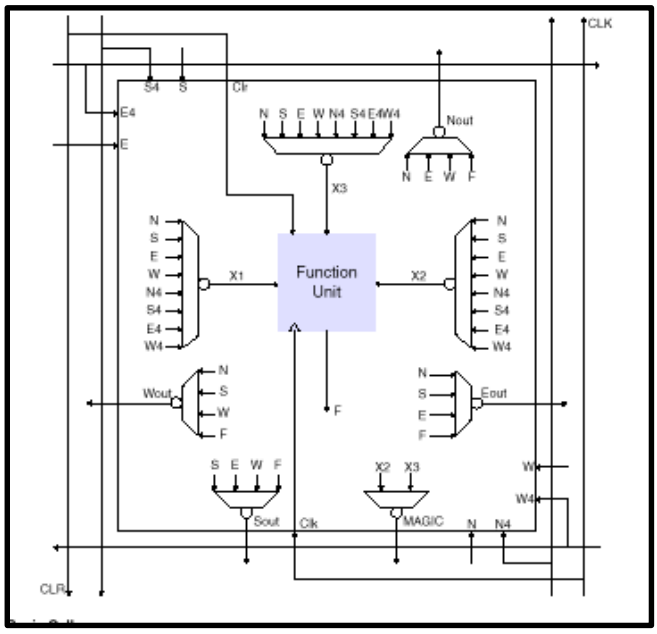

Figure 4. XC6200 Basic Cell

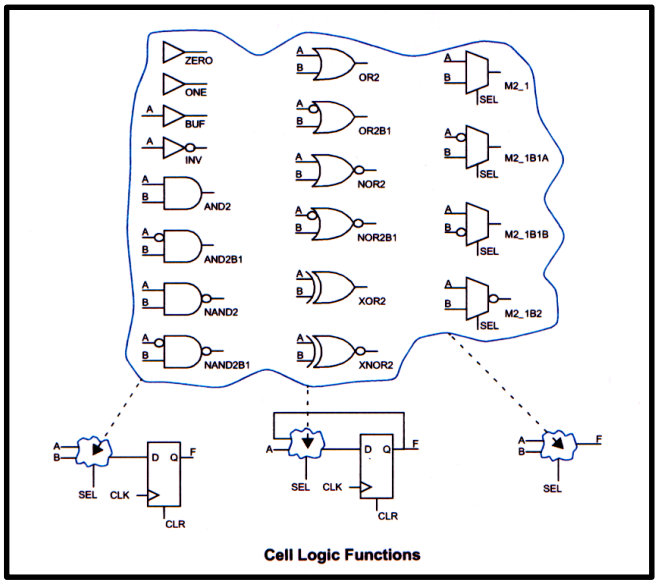

Figure 6. Cell Logic Functions

At the time of publication of this paper, a detailed analysis of the schematic implemented in the original commercial XC6200 was underway. Once a full extraction of this schematic is finished, radiation tolerant ultra-low power circuitry will be substituted in the new design for simulation, layout, and fabrication. The completion of this development program will include testing to demonstrate the power savings expected, and radiation characterization to validate the benefit of the circuit methods utilized.

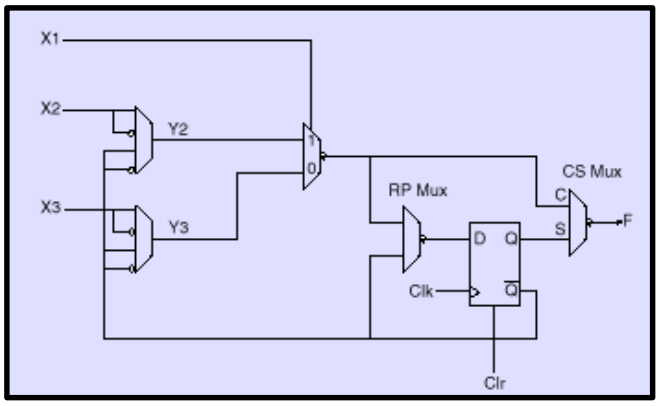

Figure 5. XC6200 Function Unit

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VII. Summary & Conclusions

We have described a new reconfigurable FPGA device that will be developed using proven radiation tolerant design methods and revolutionary ultra-low power CMOS processing that will provide significant power savings for satellite systems. The ultra-low power process is implemented in a standard commercial foundry and no process changes are required to achieve radiation tolerance required for satellite systems.

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